Verilog Generator Schema

- 5.1.7.1.4.2. Property `Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties > unconnected > oneOf > item 1`

Title: Verilog Generator Schema

Type	`object`
Required	No
Additional properties	[Any type: allowed]

Description: Default Verilog Generator Schema

Property	Pattern	Type	Deprecated	Definition	Title/Description
+ name	No	string	No	-	The name to give the generated python module
+ ip_name	No	string	No	-	The verilog name of the module
- parameters	No	object	No	-	The verilog parameters to be passed to this module, a assignment of null requires the user to provide the param. If you wish to include a apostrophe ' in a a string param you must add quotes around your string. Otherwise it will be detected as a sized int like 27'h00.
- hidden_parameters	No	object	No	-	parameters that should be populated but that shouldn't be exposed in the python module interface
+ interfaces	No	array of object	No	-	Array of dicts representing interfaces

1. Property `Verilog Generator Schema > name`

Type	`string`
Required	Yes

Description: The name to give the generated python module

2. Property `Verilog Generator Schema > ip_name`

Type	`string`
Required	Yes

Description: The verilog name of the module

3. Property `Verilog Generator Schema > parameters`

Type	`object`
Required	No
Additional properties	[Should-conform]

Description: The verilog parameters to be passed to this module, a assignment of null requires the user to provide the param. If you wish to include a apostrophe ' in a a string param you must add quotes around your string. Otherwise it will be detected as a sized int like 27'h00.

Property	Pattern	Type	Deprecated	Definition	Title/Description
-	No	string, number, integer, boolean or null	No	-	-

3.1. Property `Verilog Generator Schema > parameters > additionalProperties`

Type	`string, number, integer, boolean or null`
Required	No

4. Property `Verilog Generator Schema > hidden_parameters`

Type	`object`
Required	No
Additional properties	[Should-conform]

Description: parameters that should be populated but that shouldn't be exposed in the python module interface

Property	Pattern	Type	Deprecated	Definition	Title/Description
-	No	string, number, integer or boolean	No	-	-

4.1. Property `Verilog Generator Schema > hidden_parameters > additionalProperties`

Type	`string, number, integer or boolean`
Required	No

5. Property `Verilog Generator Schema > interfaces`

Type	`array of object`
Required	Yes

Description: Array of dicts representing interfaces

	Array restrictions
Min items	N/A
Max items	N/A
Items unicity	False
Additional items	False
Tuple validation	See below

Each item of this array must be	**Description**
interfaces items	-

5.1. Verilog Generator Schema > interfaces > interfaces items

Type	`object`
Required	No
Additional properties	[Any type: allowed]

Property	**Pattern**	**Type**	**Deprecated**	**Definition**	**Title/Description**
+ interface_name	No	string	No	-	The name to give the interface
+ type	No	string	No	-	The type name of the interface
+ side	No	enum (of string)	No	-	The side of the interface
- multi	No	array	No	-	List of strings to be substituted for ? in strings used to create the multiple interfaces

Property	Pattern	Type	Deprecated	Definition	Title/Description
- multiconnect	No	enum (of string)	No	-	Behavior if multiple interfaces connected
- interconnect_settings	No	object	No	-	Settings for an interconnect
+ ports	No	object	No	-	Contains ports and their definitions

5.1.1. Property `Verilog Generator Schema > interfaces > interfaces items > interface_name`

Type	`string`
Required	Yes

Description: The name to give the interface

5.1.2. Property `Verilog Generator Schema > interfaces > interfaces items > type`

Type	`string`
Required	Yes

Description: The type name of the interface

5.1.3. Property `Verilog Generator Schema > interfaces > interfaces items > side`

Type	`enum (of string)`
Required	Yes

Description: The side of the interface

Must be one of:

- "source"
- "sink"
- "start"
- "end"

5.1.4. Property `Verilog Generator Schema > interfaces > interfaces items > multi`

Type	`array`
Required	No

Description: List of strings to be substituted for ? in strings used to create the multiple interfaces

	Array restrictions
Min items	N/A
Max items	N/A
Items unicity	False
Additional items	False
Tuple validation	See below

Each item of this array must be	Description
multi items	-

5.1.4.1. Verilog Generator Schema > interfaces > interfaces items > multi > multi items

Type	`string or integer`
Required	No

5.1.5. Property `Verilog Generator Schema > interfaces > interfaces items > multiconnect`

Type	`enum (of string)`
Required	No

Description: Behavior if multiple interfaces connected

Must be one of:

- "false"
- "shared"
- "interconnect"

5.1.6. Property `Verilog Generator Schema > interfaces > interfaces items > interconnect_settings`

Type	`object`
Required	No
Additional properties	[Any type: allowed]

Description: Settings for an interconnect

Property	Pattern	Type	Deprecated	Definition	Title/Description

Property	Pattern	Type	Deprecated	Definition	Title/Description
- params	No	object	No	-	All key values will be passed as parameters to the interconnect
- pass_clock	No	string	No	-	clock interface to pass to the interconnect. Use the name assigned to the clock in your vgen file
- pass_reset	No	string	No	-	reset interface to pass to the interconnect. Use the name assigned to the reset in your vgen file

5.1.6.1. Property `Verilog Generator Schema > interfaces > interfaces items > interconnect_settings > params`

Type	`object`
Required	No
Additional properties	[Any type: allowed]

Description: All key values will be passed as parameters to the interconnect

5.1.6.2. Property `Verilog Generator Schema > interfaces > interfaces items > interconnect_settings > pass_clock`

Type	`string`
Required	No

Description: clock interface to pass to the interconnect. Use the name assigned to the clock in your vgen file

5.1.6.3. Property `Verilog Generator Schema > interfaces > interfaces items > interconnect_settings > pass_reset`

Type	`string`
Required	No

Description: reset interface to pass to the interconnect. Use the name assigned to the reset in your vgen file

5.1.7. Property `Verilog Generator Schema > interfaces > interfaces items > ports`

Type	`object`
Required	Yes
Additional properties	[Should-conform]

Description: Contains ports and their definitions

Property	Pattern	Type	Deprecated	Definition	Title/Description
-	No	object	No	-	-

5.1.7.1. Property `Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties`

Type	`object`
Required	No
Additional properties	[Any type: allowed]

Property	Pattern	Type	Deprecated	Definition	Title/Description
+ name	No	string	No	-	Name of the input/output wire in the module
- dir	No	enum (of string)	No	-	Direction of the wire input/output
- width	No	integer	No	-	Size of the port in bits
- unconnected	No	Combination	No	-	Behavior if port isn't connected only applies if input

5.1.7.1.1. Property `Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties > name`

Type	`string`
Required	Yes

Description: Name of the input/output wire in the module

5.1.7.1.2. Property `Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties > dir`

Type	`enum (of string)`
Required	No

Description: Direction of the wire input/output

Must be one of:

- "input"
- "output"

5.1.7.1.3. Property `Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties > width`

Type	integer
Required	No

Description: Size of the port in bits

Restrictions	
Minimum	≥ 0

5.1.7.1.4. Property Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties > unconnected

Type	combining
Required	No
Additional properties	[Any type: allowed]

Description: Behavior if port isn't connected only applies if input

One of(Option)
item 0
item 1

5.1.7.1.4.1. Property Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties > unconnected > oneOf > item 0

Type	enum (of string)
Required	No

Description: Special unconnected port behaviors

Must be one of:

- "tie_high"
- "tie_low"
- "forbidden"
- "nothing"

5.1.7.1.4.2. Property Verilog Generator Schema > interfaces > interfaces items > ports > additionalProperties > unconnected > oneOf > item 1

Type	number
Required	No

Description: Assign a custom numeric value to a port when it is left unconnected

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