CPV: A Circuit-Based Program Verifier

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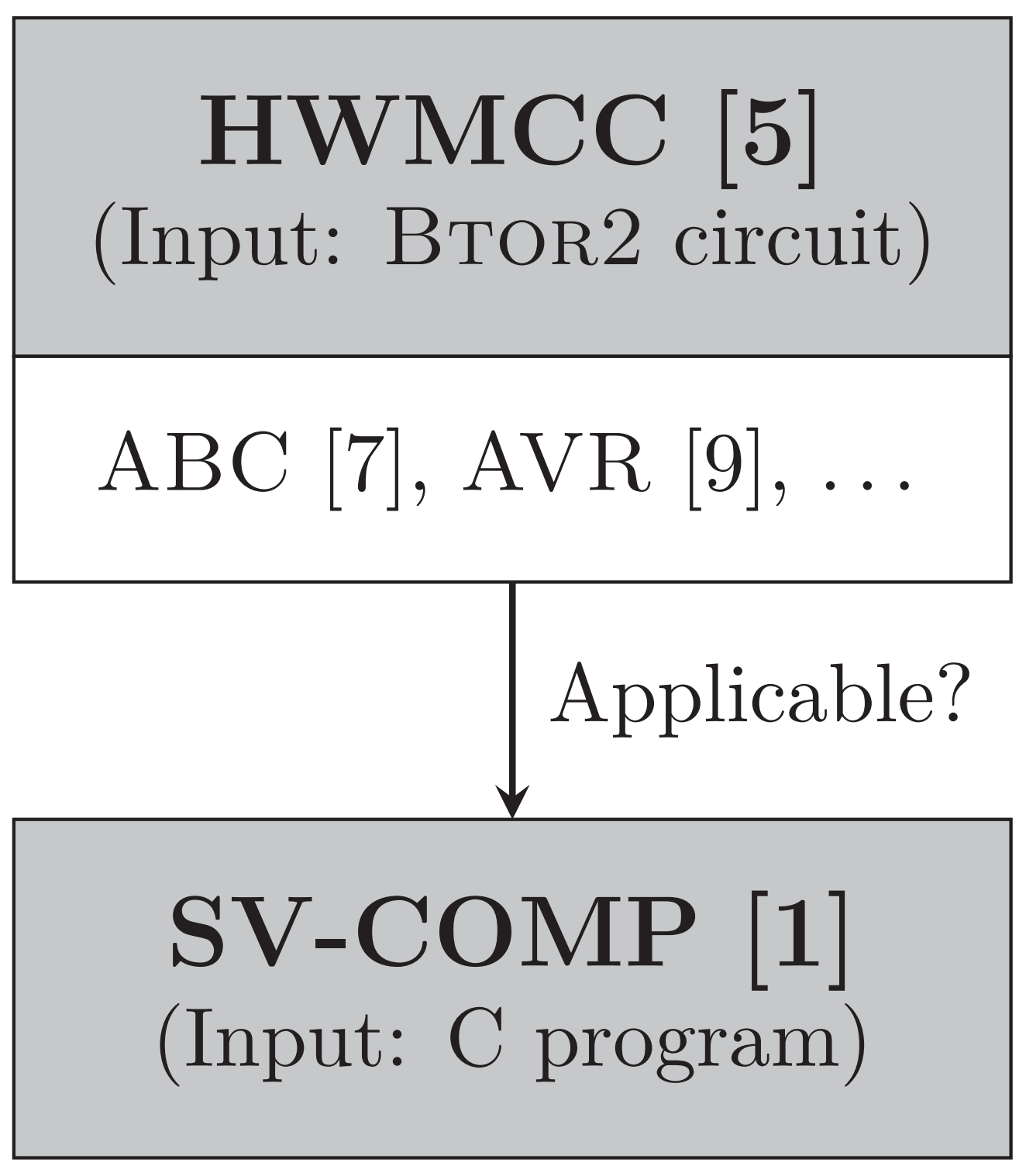
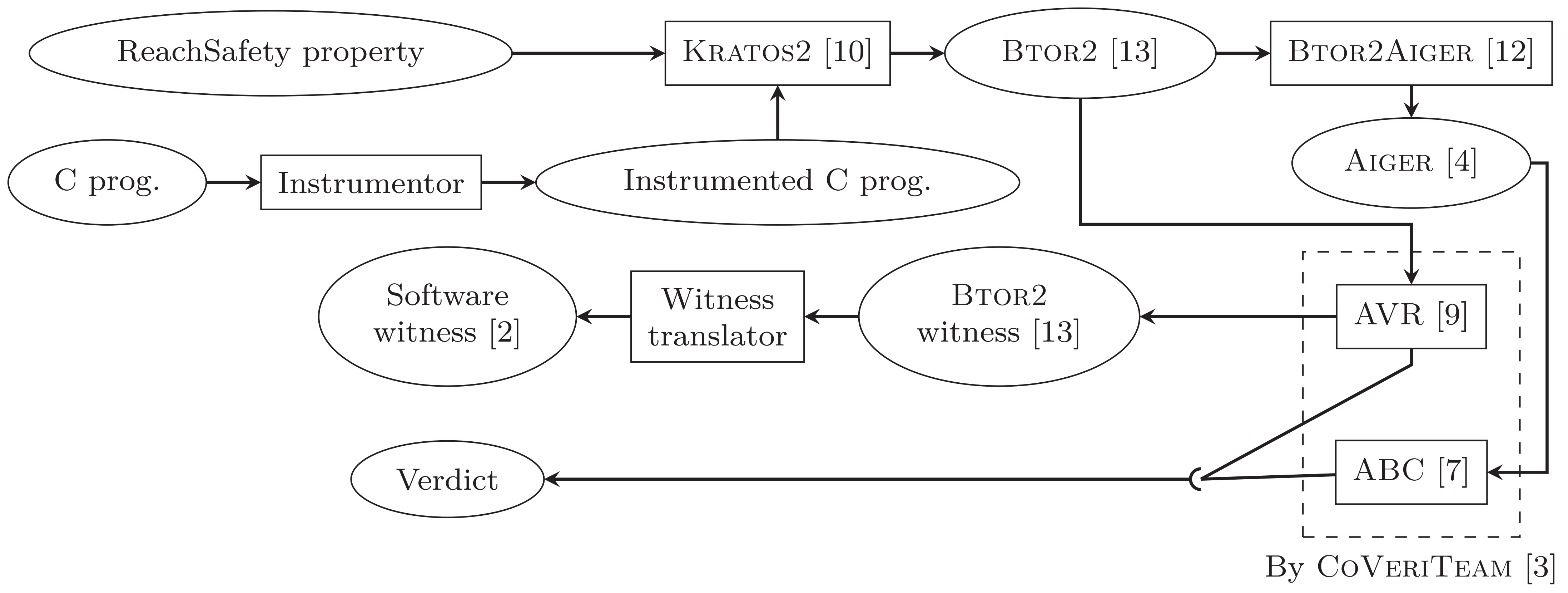
Motivation



Software Architecture

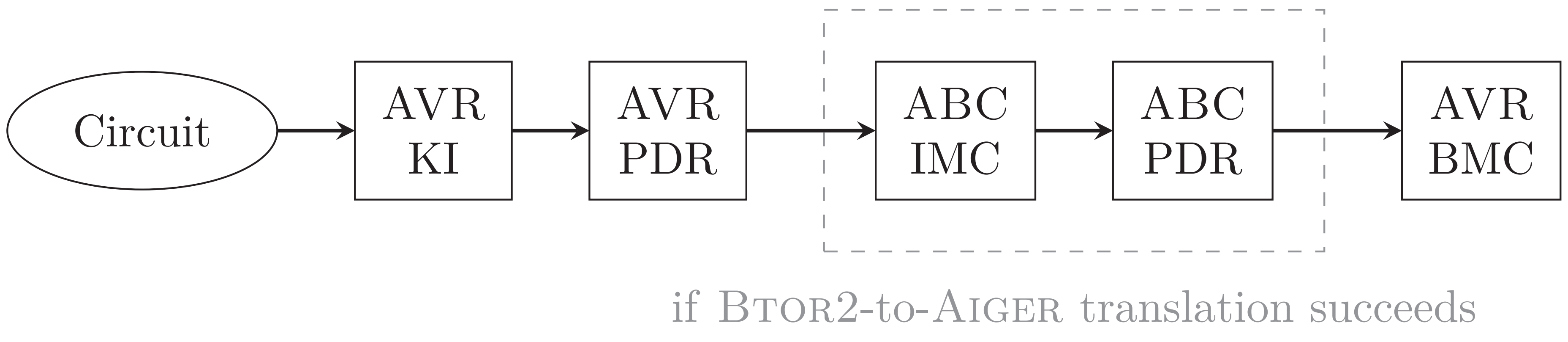


Try CPV!

Artifact DOI: `10.5281/zenodo.10063681`

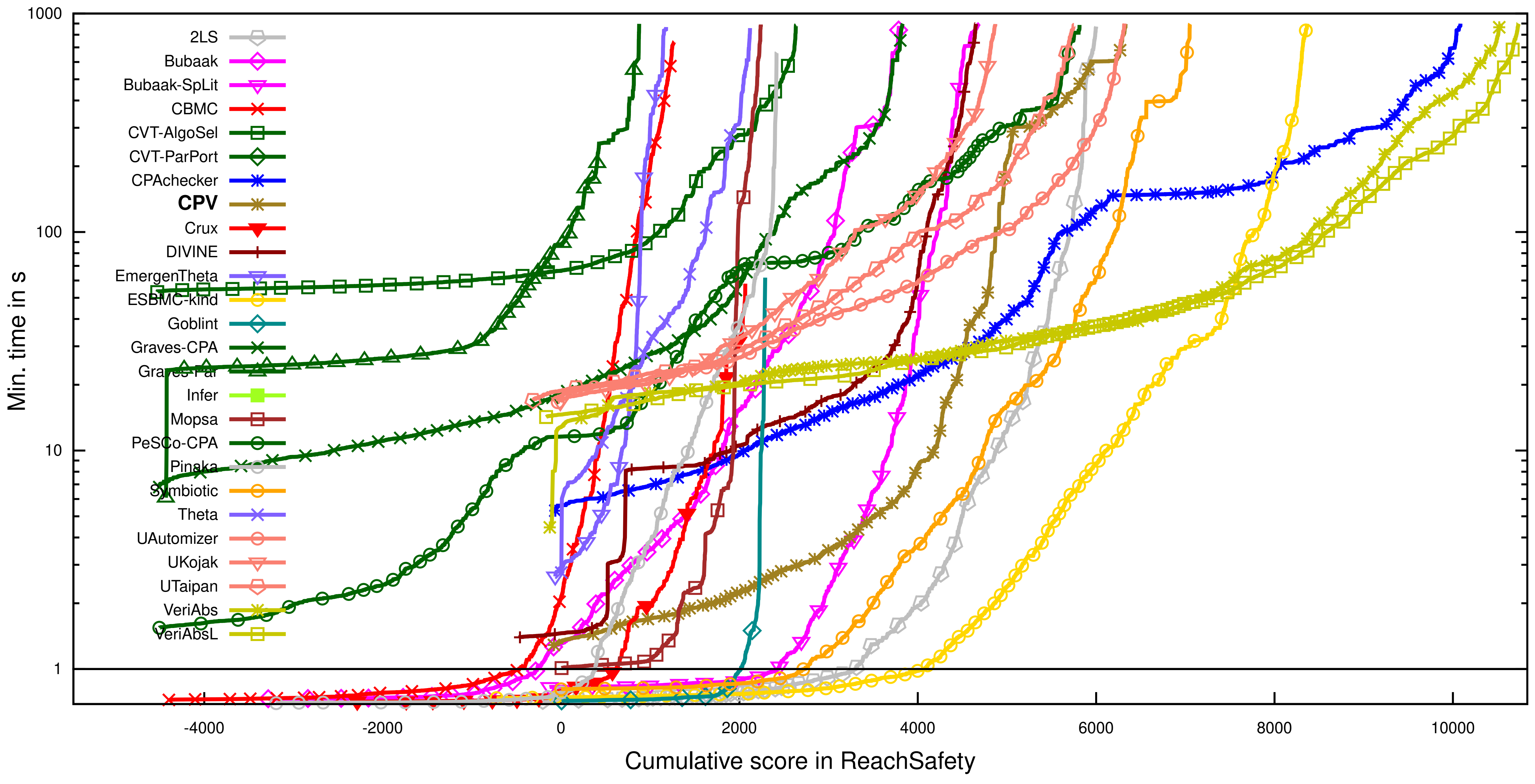
Strategy for SV-COMP 2024

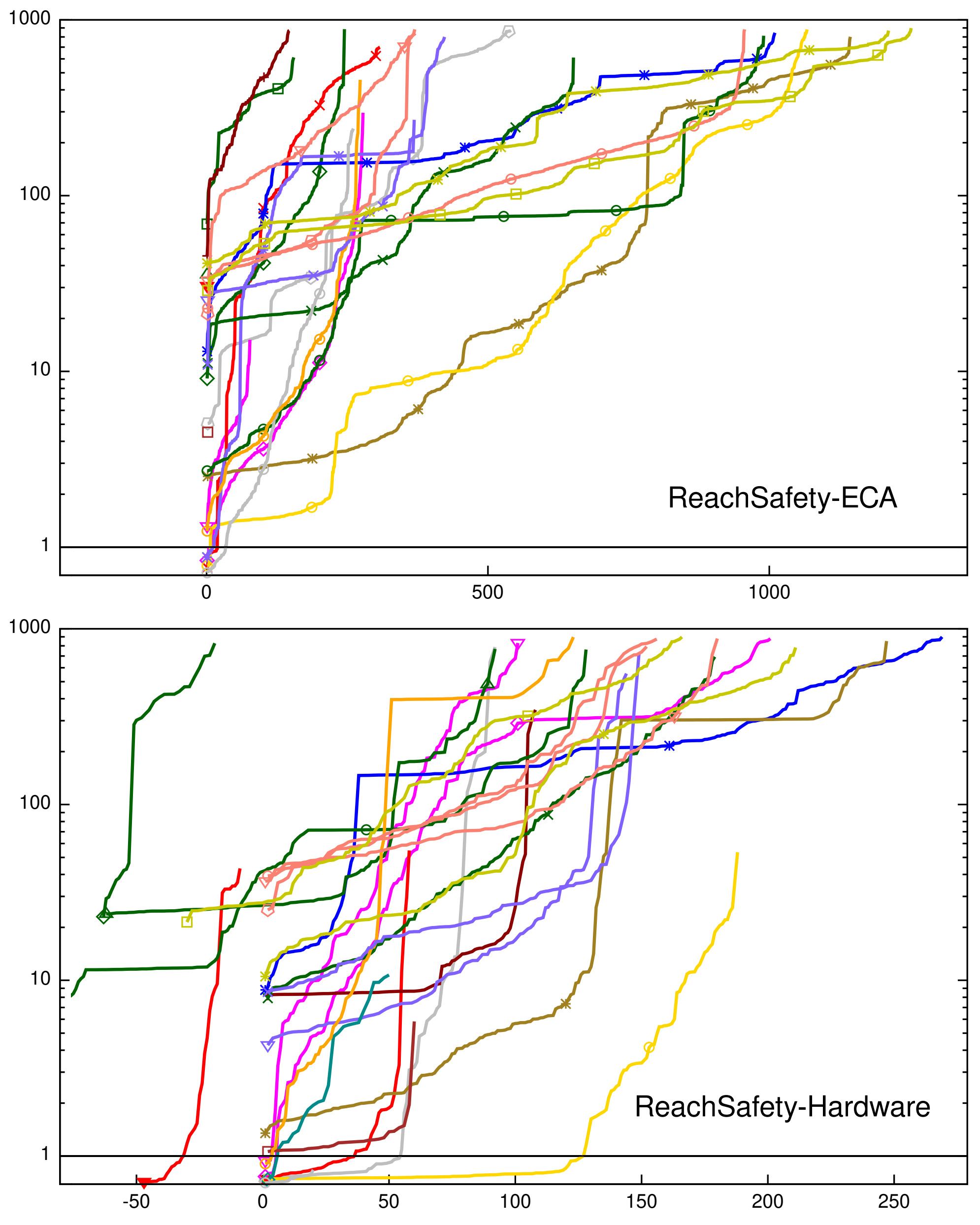
CPV runs a sequential portfolio consisting of property-directed reachability (PDR) [8], interpolation-based model checking (IMC) [11], k-induction (KI) [14], and bounded model checking (BMC) [6].



Evaluation Results at SV-COMP 2024

6th, 3rd, and 2nd place in *ReachSafety*, *ReachSafety-ECA*, *ReachSafety-Hardware*, respectively





Summary

- It is feasible to utilize sequential circuits as intermediate representations for software verification
- CPV can employ different hardware verifiers as the backend
- CPV competed well against other mature verifiers in SV-COMP
- Future work:
  - Support more verification properties (e.g., no-overflow and termination)
  - Export correctness witnesses
  - Incorporate more backend verifiers
  - Apply circuit optimization to improve the performance of verification

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